II. Objection to Drawings

The Office Action objects to the drawings under 37 CFR 1.83(a). Specifically, the Office Action objects to FIGS. 1, 2, and 4 – 16 because "the blank boxes representing the elements of the circuits have no labels." Furthermore, the Office Action states that "Applicant is required to label them with the symbols of each element or at least label them with formal functions."

Applicants have amended FIGS. 1, 2, and 4 – 16 by labeling the blank boxes corresponding to the claimed transistor devices, impedance circuits, and inverter circuits with the corresponding language. Accordingly, Applicants respectfully request that the objection to the Drawings be withdrawn.

III. Objection to the Oath/Declaration

The Office Action objects to the oath or declaration because "the post office address [is] omitted." Applicants respectfully note that the executed Oath/Declaration contains the residential address for all inventors and, therefore, is not defective merely because it fails to list a post office address. If, in the opinion of the Examiner, a new Oath/Declaration is required, please make a such a request and one will be provided.

IV. Rejections Under 35 U.S.C. §112, Second Paragraph

The Office Action rejects claims 5 – 8 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Specifically, with respect to claim 5, the Office Action states that the recitation of "an inverter" is indefinite because it is unclear in what drawing the "an inverter" is read on. As stated above and shown in red permanent ink on the separate accompanying sheet(s), Applicants amended FIG. 11 by labeling the box represented by reference numeral 1102 with the text "inverter circuit" as recited in claim 5. Accordingly, Applicants respectfully request that the rejection of claim 5 be withdrawn.

With respect to claim 6, the Office Action states that the recitation of "a second terminal" is indefinite because the connection is not complete (*i.e.*, the "a second terminal" is left dangling). The Office Action further states that the recitation of "the control signal" on lines 10 and 13 is indefinite because it is unclear whether the recitation of "the control signal" is the same as the recitation of "a control signal" on line 5. The Office Action notes that the control signals are labeled differently in the drawings, and the specification does not disclose the relationship among these control signals.

As stated above and illustrated in the attached "Annotated Version of Modified Claims to Show Changes Made," Applicants amended claim 6 by substituting the language "third terminal" with the language "second terminal" to clarify that the second transistor device has a first terminal connected to the ***second*** terminal (not the ***third*** terminal) of the first transistor device. Thus, the recitation of "a second terminal" on line 5 is not indefinite because the amended claim clarifies (as illustrated in FIGS. 12 and 13) that the second terminal of the first transistor device is connected to the first terminal of the second transistor device.

Furthermore, Applicants respectfully assert that the recitations of "the control signal" on lines 10 and 13 are not indefinite because each recitation has antecedent basis in the recitation of "a control signal" on line 5. The Office Action suggests that the control signals are labeled differently in the drawings and that the specification does not disclose the relationship among the control signals. Applicants respectfully note that it is the ***terminals*** that are labeled differently, not the ***control signals***. Therefore, the recitations of "the control signal" on lines 10 and 13 are not indefinite. It should be clear that, in accordance with the practice of claiming with proper antecedent basis, they are referring to the recitation of "a control signal" on line 5. Accordingly, Applicants respectfully request that the rejection of claim 6 be withdrawn.

Furthermore, the Office Action states that dependent claims 7 and 8 (which depend on independent claim 6) are rendered indefinite by the deficiencies of independent claim 6. Applicants respectfully request that the rejection of claims 7 and 8 be withdrawn because the underlying deficiencies in claim 6 have been corrected as described above.

Applicants also note with appreciation the Examiner's indication that claims 6 – 8 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. §112, second paragraph. For at least the reasons set forth above, the rejections to claims 6 – 8 should be withdrawn. Accordingly, Applicants request that claims 6 – 8 be placed in condition for allowance.

V. Claims 1 and 2 are Patentable Over U.S. Patent No. 5,204,562 to *Pace*

The Office Action rejects claims 1 and 2 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,707,834 to *Pace* ("the '562 patent").

Independent claim 1 has been amended to define more clearly the present invention. Prior to amendment, independent claim 1 recited that the circuit connected to the third switch

node and the third terminal of the transistor device had "an impedance configured to reduce the parasitic capacitance of the transistor device." Independent claim 1 has been amended to clarify that the characteristic impedance of the circuit should be high enough to prevent the third switch node from functioning as an AC ground to the transistor device. Support for this clarification is in the original specification at page 8, ll. 4 – 14.

In contrast to independent claim 1, the '562 patent cited by the Examiner does not disclose, teach, or suggest the use of an impedance high enough to prevent the third switch node from functioning as an AC ground to the transistor device. Rather, the '562 patent discloses a current boost circuit 32 configured to provide a ***low impedance*** path between two terminals of a MOSFET in order to rapidly discharge the gate capacitance of the MOSFET. Col. 2, ll. 35 – 40. Therefore, the ***high impedance*** circuit of the claimed invention is patentably distinct from the ***low impedance*** current boost circuit 32 disclosed in the '562 patent.

Furthermore, in addition to the impedance difference between the claimed invention and the current boost circuit 32 disclosed in the '562 patent, the impedance circuit in the claimed invention is used for an entirely different purpose. The impedance circuit in the claimed invention uses a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch. Current boost circuit 32, however, uses a low impedance to rapidly discharge the gate capacitance of the MOSFET. Therefore, not only is the claimed invention structurally different than the current boost circuit 32 disclosed in the '562 patent, but it is also designed for a completely different purpose.

Independent claim 1 contains the limitation of using a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch. Accordingly, and for at least this reason, Applicants respectfully

submit that independent claim 1 patently defines over the '562 patent and, therefore, is in condition for allowance. Furthermore, because independent claim 1 is believed to be allowable over the prior art of record, dependent claim 2 (which depends from independent claim 1) is allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 1 and 2 in condition for allowance.

VI. Claims 1 and 2 are Patentable Over U.S. Patent No. 6,281,737 to *Kuang et al.*

The Office Action also rejects claims 1 and 2 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,281,737 to *Kuang et al.* ("the '737 patent").

As stated above, independent claim 1, as amended, contains the limitation of using a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch. In contrast, the '737 patent does not disclose, teach, or suggest the use of an impedance high enough to prevent the third switch node from functioning as an AC ground to the transistor device. Rather, the '737 patent discloses body-charge control circuitry comprising an inverter, which is designed to provide an output voltage that tends to turn off the body-charge control FET and electrically isolate the body from the sink. Col. 2, ll. 30 – 34. The inverter circuit provides the effect of lowering the threshold voltage in the FET during activation and achieving the benefit of no charge buildup in a grounded body FET during deactivation. Col. 4, 26 – 31.

Thus, the '737 patent does not disclose, teach, or suggest anything about the impedance of the body-charge control circuitry. Furthermore, the claimed invention is used for an entirely different purpose than the body-charge control circuitry disclosed in the '737 patent. As stated above, the impedance circuit in the claimed invention uses a sufficiently

high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch. The circuitry disclosed in the '737 patent, however, is designed to lower the threshold voltage in the FET during activation and provide no charge buildup in a grounded body FET during deactivation. Col. 4, 26 – 31.

Accordingly, and for at least these reasons, Applicants respectfully submit that independent claim 1 patently defines over the '737 patent and, therefore, is in condition for allowance. Furthermore, because independent claim 1 is believed to be allowable over the prior art of record, dependent claim 2 (which depends from independent claim 1) is allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 1 and 2 in condition for allowance.

VII. Claims 3 and 4 are Patentable Over U.S. Patent No. 5,223,751 to *Simmons et al.*

The Office Action rejects claims 3 and 4 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,223,751 to *Simmons et al.* ("the '751 patent").

Applicants respectfully assert that this rejection should be withdrawn because the '751 patent does not teach, disclose, or suggest all of the limitations of independent claim 3. Independent claim 3 is directed at a circuit for implementing a transistor-based ***switch***. Independent claim 1 contains the limitation of ***first and second switch nodes***. In addition, independent claim 1 contains the limitation of a transistor device having a terminal configured to receive a control signal for controlling the electrical connectivity between two other terminals. Thus, independent claim 1 includes a transistor device and corresponding circuitry for implementing a ***switch***.

In contrast, the '751 patent does not disclose, teach, or suggest a transistor circuit for implementing a ***switch***, which comprises ***first and second switch nodes***. Furthermore, the '751 patent does not disclose, teach, or suggest the limitation of a transistor device having a terminal configured to receive a control signal for controlling the electrical connectivity between the other two terminals. In fact, the '751 patent does not make any reference to the use of a transistor circuit for implementing a switch. Rather, the '751 patent discloses a two-stage logic level shifter for reducing static current drain.

Accordingly, and for at least this reason, Applicants respectfully submit that independent claim 3 patently defines over the '751 patent and, therefore, is in condition for allowance. Furthermore, because independent claim 3 is believed to be allowable over the prior art of record, dependent claim 4 (which depends from independent claim 3) is allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 3 and 4 in condition for allowance.

VIII. Claims 3 – 5 are Patentable Over U.S. Patent No. 5,532,630 to *Waggoner et al.*

The Office Action rejects claims 3 - 5 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,532,630 to *Waggoner et al.* ("the '630 patent").

Applicants respectfully assert that this rejection should be withdrawn because the '630 patent does not teach, disclose, or suggest all of the limitations of independent claim 3. Independent claim 3 is directed at a circuit for implementing a transistor-based ***switch***. Independent claim 1 contains the limitation of ***first and second switch nodes***. In addition, independent claim 1 contains the limitation of a transistor device having a terminal configured to receive a control signal for controlling the electrical connectivity between two

other terminals. Thus, independent claim 1 includes a transistor device and corresponding circuitry for implementing a ***switch***.

In contrast, the '630 patent does not disclose, teach, or suggest a transistor circuit for implementing a ***switch***, which comprises ***first and second switch nodes***. Furthermore, the '630 patent does not disclose, teach, or suggest the limitation of a transistor device having a terminal configured to receive a control signal for controlling the electrical connectivity between the other two terminals. In fact, the '630 patent does not make any reference to the use of a transistor circuit for implementing a switch. Rather, the '630 patent discloses the use of complementary bus keeper transistors in a bidirectional input/output buffer; not a ***switch***.

Accordingly, and for at least this reason, Applicants respectfully submit that independent claim 3 patently defines over the '630 patent and, therefore, is in condition for allowance. Furthermore, because independent claim 3 is believed to be allowable over the prior art of record, dependent claims 4 and 5 (which depend from independent claim 3) are allowable as a matter of law for at least the reason that they contain all features and elements of the corresponding independent claim. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Accordingly, the Examiner is respectfully requested to withdraw this rejection and place claims 3 - 5 in condition for allowance.

CONCLUSION

In light of the foregoing remarks and for at least the reasons set forth above, Applicant respectfully submits that all rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1 - 8 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington D.C. 20231, on 2-7-2007.

Signature

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

1. (amended once) A transistor circuit for implementing a switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a transistor device having a first terminal electrically communicating with the first switch node, a second terminal connected to the second switch node, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a third switch node for receiving the control signal; and

a circuit connected to the third switch node and the third terminal of the transistor device, the circuit having [an] a sufficiently high impedance to prevent the third switch node from functioning as an alternating current (AC) ground during operation of the switch [configured to reduce the parasitic capacitance of the transistor device].

6. (amended once) A transistor circuit for implementing a differential switch, comprising:

a first switch node configured to connect to an external circuit;

a second switch node configured to connect to the external circuit;

a first transistor device having a first terminal connected to the first switch node, a second terminal, and a third terminal configured to receive a control signal that controls the electrical connectivity between the first terminal and the second terminal;

a second transistor device having a first terminal connected to the [third] second terminal of the first transistor device, a second terminal connected to the second switch node, and a third terminal configured to receive the control signal; and

a third transistor device having a first terminal connected to the first terminal of the first transistor device, a second terminal connected to the second terminal of the second transistor device, and a third terminal configured to receive the control signal.